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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/683,588	10/14/2003	Nobuyoshi Takehara	00862.023271.	2946

5514 7590 03/08/2005

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EXAMINER	
NGUYEN, MINH T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 03/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/683,588	TAKEHARA, NOBUYOSHI	
	Examiner	Art Unit	
	Minh Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 October 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 2/22/05 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 4,481,434, issued to Janutka.

As per claim 1, Janutka discloses a gate driving circuit (Fig. 1), comprising:

a direct current power source (the source to power the circuit);

a driving source (VG) for outputting a high and low signal (column 2, lines 12-19, high: apply, low: remove);

a main switch device (4), the gate (G) receiving the signal (VG) from the driving source (VG) at node 10;

a load (connected to node 6, not shown, however, it must be there because FET 4 of the Janutka circuit functioned as a switch), when FET 4 is ON, the current flows through the drain and source of the FET and through the load, i.e., the load is energized;

a reverse current blocking means (diode 18), connected as recited, functioned as recited because it is a diode; and

a regenerative means (12), connected between the gate and a low potential side of the direct current power source and functioned as recited (column 2, lines 12-30, the description of the operation of the circuit clearly meets the recited function, also see the title to confirm the function).

The limitation recited on the last three lines is inherently met because the Janutka gate driver circuit using regenerative technique, i.e., otherwise the main switch (FET 4) cannot be turned OFF upon regeneration.

Janutka does not explicitly disclose the regenerative means connected between the gate and a high potential side of the direct current power source as called for in the claim (Janutka discloses the connection between the gate and a low potential side of the direct current power source).

However, as recognized by a person average skilled in the art, NPN and PNP transistors are interchangeable and art recognized equivalent provided properly biasing. Further, properly biasing PNP or NPN transistors are taught in every basis electronics textbooks.

It would have been obvious to one skilled in the art at the time of the invention was made to adjust the connection of the Janutka regenerative means to the high potential side of the direct current power source instead of the low potential side of the direct current power source by replacing the PNP transistor 14 by an NPN transistor.

The motivation and/or suggestion for doing so would have been obvious since it has been well-known that by rearranging the connections and parts of electronics component in a circuit, the EMI problem can be reduced, and further, reducing EMI problems in a circuit are clearly desirable.

As per claim 2, the Janutka main switch 4 is clearly an NFET.

As per claim 3, the recited diode reads on diode 18.

As per claim 4, Janutka discloses the regenerative means include a PNP transistor but he does not explicitly disclose a MOSFET as called for in the claim.

However, replacing a PNP transistor by an equivalent MOSFET is seen as an obvious replacement by a person skilled in the art at the time of the invention was made for the obvious motivation which is also well-known in the art, i.e., bipolar consumes more power but speedier than MOSFET whereas MOSFET consumes little power and slower. The choice is clear by a person average skilled in the art, i.e., depending on a particular application.

As per claim 5, the claim is rejected for the same reasons and motivation discussed in claim 1.

As per claims 6-8, the recited limitations are merely intended uses of a gate driver circuit, and since, the Janutka's gate driver clearly can be used with such a load and/or for performing DC/AC conversion and/or with any direct power source, the recited limitations are met.

Response to Arguments

3. Applicant's argument filed on 2/22/05 has been fully considered but it is not persuasive.

The applicant argues that the proposed modification would result the FET 4 could not be turned off since a high potential voltage would always be applied to the FET gate.

The argument is not found persuasive because it is believed that the proposed modification does not prevent the FET 4 from being turn off as argued by the applicant. Specifically, by applying an appropriate voltage to the gate terminal 10 of the circuit, FET 10 would be turned OFF.

However, if the applicant strongly believes that the proposed modification would result the FET 4 could not be turned off since a high potential voltage would always be applied to the FET gate as argued, the applicant is invited to file for the record an affidavit under 37 CFR 1.132 traversing the rejection for the specific reason which is *the proposed modification would result in the FET 4 could not be turned off since a high potential voltage would always be applied to the FET gate* to overcome the rejection.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is **571-272-1748**. The examiner can normally be reached on Monday, Tuesday, Thursday, Friday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

3/4/05

Minh Nguyen
Primary Examiner
Art Unit 2816